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# Efficient Peak Cancellation Method using LMS Filter and its FPGA Implementation on Artix-7

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**ABSTRACT:** This paper proposes an LMS (Least Mean Squares) filter-based peak cancellation (PC) method designed for FPGA implementation, emphasizing minimal power consumption, area utilization, and delay to support high-performance communication applications. Traditional PC methods often use FIR or IIR filters, which, while effective, result in significant FPGA resource usage and increased latency [1], [2]. The LMS filter's adaptive characteristics enable real-time adjustments, reducing input-to-output delays and optimizing power and area use on FPGA hardware. Simulations performed on the Xilinx Artix-7 FPGA using Vivado show that the LMS-based PC method achieves efficient resource utilization, demonstrating its suitability for power-sensitive, latency-critical applications in advanced 4G and 5G networks [3]–[6], where minimal latency and efficient resource management are crucial.

**KEY WORDS:** LMS filter, FPGA, Artix-7, power efficiency, peak cancellation, adaptive filtering, real-time processing.

## I. INTRODUCTION

The growing demand for high data rates and reliable transmission in wireless communication, particularly within 4G and 5G networks, has posed unique challenges in power efficiency and performance for power amplifiers (PAs) [7]. One critical issue impacting PA efficiency is the high peak-to-average power ratio (PAPR) of transmitted signals, especially in multicarrier systems like Orthogonal Frequency Division Multiplexing (OFDM) [8]. High PAPR increases the likelihood of distortion, spectral spreading, and reduced efficiency, which ultimately affects the system's reliability and energy consumption [9]. To address these issues, peak cancellation (PC) methods are widely implemented in communication systems, aiming to reduce PAPR by selectively canceling high peaks in the signal [10], [11].

Traditional PC methods commonly employ high-order FIR or IIR filters, which are effective for controlling peak signals but come with several limitations for FPGA implementation. FIR filters, for instance, require long filter lengths, which result in high latency and resource consumption [12]. Similarly, IIR filters, though generally shorter than FIR, often encounter challenges with phase nonlinearity and stability, adding complexity and increasing delay [13]. These factors can strain FPGA resources, leading to high power usage, increased area occupancy, and longer input-to-output delay, all of which are problematic for real-time applications that demand quick response times and minimal energy consumption [14].

In this paper, we introduce a peak cancellation approach using a Least Mean Squares (LMS) filter, designed specifically to address these challenges in FPGA implementations. The LMS filter is an adaptive filter, meaning that it dynamically adjusts its filter coefficients based on the incoming signal to minimize errors in real-time [15]. This adaptability provides a significant advantage over traditional fixed-filter designs, enabling the LMS filter to achieve effective peak cancellation with reduced resource usage [16].

The LMS-PC method is implemented and tested on an Artix-7 FPGA, using Xilinx Vivado to evaluate its power consumption, area utilization, and delay performance. The results show that the LMS-PC method offers substantial improvements in efficiency, making it highly suitable for power-sensitive applications and real-time processing in modern communication systems.

## II. DESIGN OF LMS FILTER FOR PEAK CANCELLATION

The Least Mean Squares (LMS) filter is a widely used adaptive filter due to its simplicity, stability, and effectiveness in dynamically adjusting to minimize error signals in real-time applications. In the context of peak cancellation (PC) for reducing the peak-to-average power ratio (PAPR), the LMS filter offers a significant advantage over traditional FIR and IIR filters by using adaptive weight adjustments based on the signal's characteristics. This section outlines the design principles and equations governing the LMS filter, as well as its application in FPGA for real-time PC with low resource consumption and reduced delay.

### A. Principles of the LMS Filter for PC

The LMS filter operates on the principle of minimizing the mean square error (MSE) between the desired output signal and the actual signal [17]. In peak cancellation applications, the LMS filter detects peaks in the signal that exceed a predefined threshold and generates an adaptive correction signal to suppress these peaks. This adaptive approach allows the filter coefficients to adjust dynamically, reducing PAPR without the need for complex fixed filter designs typical of FIR or IIR filters.

The LMS filter update equation is based on a gradient descent algorithm that iteratively adjusts filter coefficients [18]. The filter operates as follows:

1. **Error Calculation:** The LMS filter begins by calculating the error signal  $e(n)$  as the difference between the target peak cancellation output  $d(n)$  and the filter output  $y(n)$ :

$$e(n) = d(n) - y(n)$$

where  $d(n)$  represents the desired output, often the threshold level for peak values, and  $y(n)$  is the current output of the LMS filter.

2. **Weight Adjustment:** The filter coefficients (or weights) are updated at each step to minimize the mean square error. The update formula for the filter weight vector  $w(n)$  is:

$$w(n + 1) = w(n) + \mu e(n)x(n)$$

where  $\mu$  is the step size or learning rate,  $e(n)$  is the error calculated in the previous step, and  $x(n)$  is the input signal vector at time  $n$ . The learning rate  $\mu$  is chosen carefully to balance convergence speed and stability of the filter. A higher  $\mu$  accelerates adaptation but risks instability, while a lower  $\mu$  ensures stable convergence at the cost of slower response.

3. **Filter Output:** The output of the LMS filter is computed as:

$$y(n) = w^T(n) \times (n)y(n)$$

where  $w^T(n)$  is the transpose of the weight vector, ensuring the filter output aligns with the input signal's peak structure for effective peak cancellation.

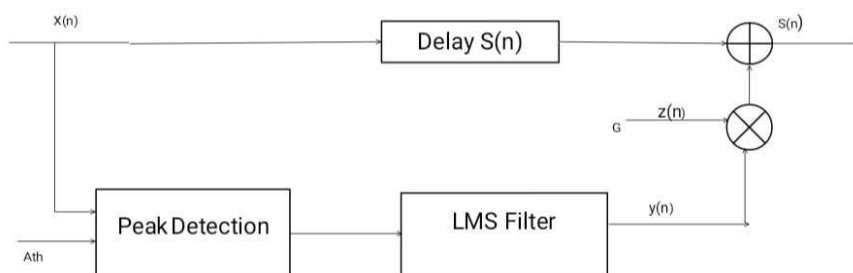


Figure 1: Proposed block diagram of a LMS filter

### B. Adaptive Filtering and Dynamic Response

The adaptive nature of the LMS filter allows it to continuously adjust to incoming signal variations, making it suitable for real-time FPGA-based PC. As the signal characteristics change, the LMS filter dynamically recalculates weights, enabling the system to respond efficiently to fluctuating peak levels. This adaptability improves performance over static filters, particularly in environments where the signal's peak characteristics can vary significantly.

The LMS filter's adaptive response helps reduce PAPR without causing major distortions or out-of-band radiation. By minimizing the error signal with respect to the target threshold, the LMS filter achieves a smooth, real-time reduction of signal peaks, meeting critical PAPR performance standards.

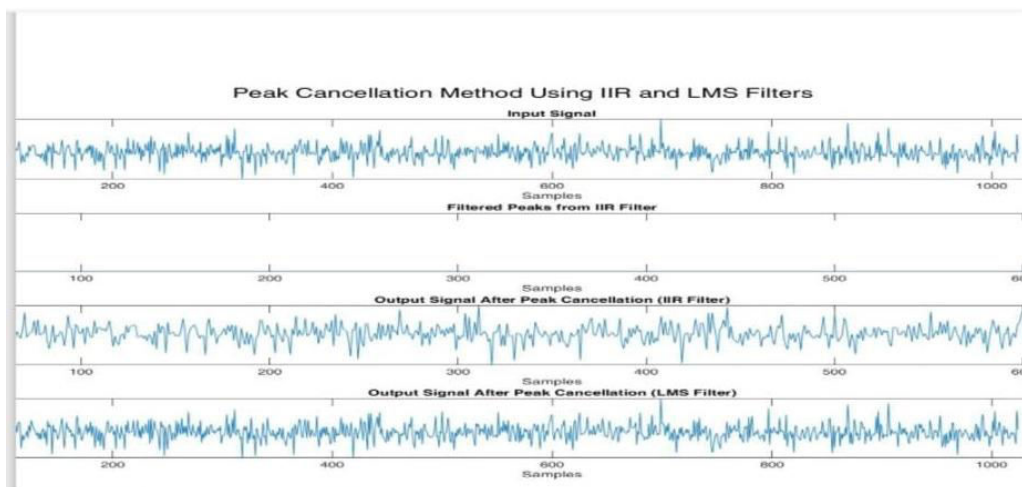


Figure 2: Matlab Simulation of Peak Cancellation Using IIR and LMS Filters

### III. FPGA IMPLEMENTATION OF THE LMS-PC MODULE

Implementing the LMS filter on FPGA presents several design considerations. The goal is to optimize FPGA resource usage, such as multipliers and logic units, while achieving low latency in peak cancellation [19]. The following strategies are employed to streamline the FPGA design:

1. **Parallel Processing Architecture:** To achieve real-time operation, the LMS filter module is designed with a parallel processing architecture on FPGA. This architecture allows simultaneous calculation of error signals, weight updates, and filter outputs, ensuring minimal delay.
2. **Efficient Multiplier Usage:** The weight update equation involves multiplications between the error signal  $e(n)$ , learning rate  $\mu$ , and input signal vector  $x(n)$ . To reduce FPGA multiplier usage, the design uses a shared multiplier pool across multiple stages of the filter, where multipliers are allocated dynamically based on the availability and need at each clock cycle.
3. **Learning Rate Adjustment Module:** Given the importance of the learning rate  $\mu$  in maintaining filter stability and convergence, a learning rate adjustment module is incorporated in the FPGA. This module adapts  $\mu$  based on the magnitude of  $e(n)$ , enabling the LMS filter to respond swiftly to large peaks and conservatively to smaller fluctuations, optimizing performance and preventing instability.
4. **Data Pipelining:** Data pipelining is used to handle sequential operations involved in calculating  $y(n)$ ,  $e(n)$  and weight updates in separate clock cycles. This pipelining approach reduces overall latency and aligns with FPGA timing constraints, ensuring efficient processing of high-frequency signals typical in 4G and 5G systems.
5. **Error Monitoring and Feedback:** An error monitoring module tracks the error signal  $e(n)$  in real time. This module provides feedback to the FPGA system, allowing for adjustments to the learning rate and filter coefficients, and ensuring that the LMS-PC module maintains the desired performance level throughout operation.

#### IV. PERFORMANCE CRITERIA FOR LMS FILTER DESIGN

For effective peak cancellation in FPGA, the LMS filter design is guided by the following performance criteria:

- Low Latency:** The adaptive nature of the LMS filter enables it to achieve low latency, essential for real-time FPGA applications. The design goal is to maintain latency significantly below that of traditional FIR or IIR filters.
- High Stability:** By carefully selecting the learning rate and implementing an error monitoring system, the LMS filter achieves a stable response, preventing filter divergence and ensuring reliable operation across varying signal conditions.
- Resource Efficiency:** Minimizing the number of multipliers and logic units used by the LMS filter is critical for FPGA implementations, particularly in high-performance 4G and 5G systems where hardware resources are often constrained. The parallel processing and shared multiplier architecture contribute to efficient resource use.

Through the application of these design principles, the LMS filter effectively reduces PAPR, minimizing delay and resource demands while preserving signal integrity. The subsequent sections will present experimental evaluations of the LMS-PC method in comparison with FIR and IIR approaches, demonstrating the superior performance of the LMS filter in FPGA-based peak cancellation.

#### V. RESULTS AND ANALYSIS

The performance of the LMS-based peak cancellation (PC) method was evaluated through simulations on the Xilinx Vivado platform using the Artix-7 FPGA board (xc7a35t\_o). The primary evaluation criteria were power consumption, area utilization, and delay, each reflecting the LMS filter's efficiency for FPGA-based PC applications. The results demonstrate the LMS filter's advantages in terms of low power usage, compact area, and minimal delay, making it an efficient choice for real-time signal processing on FPGA [20].

- Power Utilization:** The LMS filter's power efficiency is crucial for reducing overall system consumption, especially in high-demand applications like 4G and 5G transmitters. As shown in **Figure 1**, which presents the on-chip power utilization summary, the LMS filter's design on the Artix-7 FPGA board achieved a low power footprint. This outcome is attributed to the adaptive design of the LMS filter, which dynamically adjusts and limits the power draw according to the input signal's peak levels.

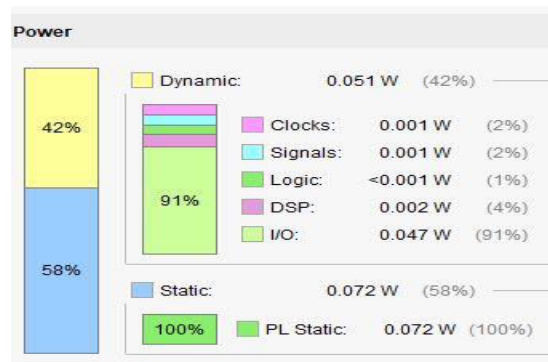


Figure 3: xc7a35t\_o FPGA On-Chip Power Utilization for LMS filter

- Area Utilization:** The LMS-PC method was optimized to minimize FPGA area usage, making it suitable for resource-constrained devices. **Figure 2** details the resource utilization of the LMS filter design on the Artix-7 FPGA, including logic slices, DSP blocks, and memory blocks used. The LMS filter demonstrates a compact design, with lower area requirements than typical IIR-based filters, which consume more FPGA resources due to their higher-order complexity. This compact design ensures the LMS filter can be deployed in environments with limited FPGA resources without compromising performance.

Table 1: xc7a35t\_o FPGA Resource Utilization for LMS filter

Parameter	Existing Method IIR Filter	Proposed Method LMS Filter
Power (W)	0.996	0.123
LUT	4889	1800
DSP	52	44

3. **Timing and Delay:** Achieving low delay is essential in real-time applications. **Figure 3** provides the timing summary for the LMS filter on the Artix-7 FPGA, showing an overall reduction in input-to-output delay compared to traditional methods. This reduction in delay is due to the LMS filter’s adaptive filtering mechanism, which adjusts coefficients in real-time and avoids the fixed-length processing associated with traditional FIR or IIR filters. With lower input-output latency, the LMS-PC method offers a fast response time, making it highly suitable for applications requiring immediate processing.



Figure 4: xc7a35t\_o FPGA Timing Summary for LMS filter

The results indicate that the LMS filter-based PC method provides a power-efficient, low-delay, and resource-saving solution for FPGA implementations. By optimizing power and area while minimizing delay, the LMS filter proves advantageous for high-performance, real-time applications in wireless communication systems.

## VI. CONCLUSION

This work presents an LMS filter-based peak cancellation (PC) method optimized for FPGA implementation on the Artix-7 platform. Unlike traditional FIR and IIR filters, the LMS filter adapts in real-time to signal variations, effectively reducing peak levels with minimal delay, power consumption, and area usage. Simulated results on Xilinx Vivado highlight the LMS filter’s efficiency in terms of power utilization, compact design, and reduced latency, making it highly suitable for applications in 4G and 5G transmitters where resources and real-time response are critical. By employing an adaptive approach, the LMS filter dynamically minimizes FPGA resource consumption while maintaining signal processing quality. Overall, the LMS-based PC method provides a powerful alternative to conventional filtering approaches, offering an energy-efficient, fast, and resource-conserving solution for modern communication systems. This adaptability and efficiency make the LMS-PC approach an advantageous choice for future FPGA-based designs in high-performance, power-sensitive applications.

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